IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant | : Masaharu Nagai et al. | Art Unit | : 1756 |
| Serial No. | : 10/694,986 | Examiner | : Daborah Chacko Davis |
| Filed | : October 29, 2003 | Confirmation No.: | 5334 |
| Title | : METHOD FOR REMOVING RESIST PATTERN AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE | | |

**MAIL STOP AMENDMENT**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants request consideration of the references listed on the attached PTO-1449 form. Under 37 C.F.R. § 1.98 (a)(2)(ii), only copies of foreign patent documents and/or non-patent literature are enclosed. Copies of any listed U.S. patents or U.S. patent application publications can be provided upon request.

This statement is being filed after a first Office action on the merits, but before receipt of a final Office action or a Notice of Allowance. A check for $180 in payment of the late submission fee of §1.17(p) is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: March 3, 2006

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| Substitute Form PTO-1449 (Modified) | U.S. Department of Commerce Patent and Trademark Office | Attorney's Docket No. 12732-171001 | Application No. 10/694,986 |
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| **Information Disclosure Statement by Applicant** (Use several sheets if necessary) | | Applicant Masaharu Nagai et al. | |
| (37 CFR §1.98(b)) | | Filing Date October 29, 2003 | Group Art Unit 1756 |



## U.S. Patent Documents

| Examiner Initial | Desig. ID | Document Number | Publication Date | Patentee | Class | Subclass | Filing Date If Appropriate |
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## Foreign Patent Documents or Published Foreign Patent Applications

| Examiner Initial | Desig. ID | Document Number | Publication Date | Country or Patent Office | Class | Subclass | Translation Yes | Translation No |
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## Other Documents (include Author, Title, Date, and Place of Publication)

| Examiner Initial | Desig. ID | Document |
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| | AQ | Hatano et al., "A Novel Self-aligned Gate-overlapped LDD Poly-Si TFT with High Reliability and Performance", IEDM 97; Technical Digest of International Electron Devices Meeting, December 7, 1997, pp. 523-526. |
| | AR | Final Office Action dated December 06, 2005 for U.S. Serial No. 10/405,908 (Your Ref.: 12732-150001, Our Ref.: US6362) |
| | AS | |
| | AT | |

| Examiner Signature | Date Considered |
|---|---|
| EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | |